Power Electronics and Drives
Volume 9(44), 2024 DOI: 10.2478/pead-2024-0014

Power Electronics and Drives

Minimisation of AC Grid Side Input Power Factor Angle for Three-phase AC to Three-phase AC Matrix Converter under Varying Load

Research paper

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Received: 22 December 2023; Accepted: 29 February 2024

Abstract: Minimisation of AC grid side input power factor angle for a 'matrix converter (MC)' improves the efficiency of the grid. Input volt-ampere requirement is minimum if the current drawn by the 'MC' is sinusoidal and input displacement power factor (IDPF) is unity. A MC is inherently capable of maintaining a unity displacement power factor (UDPF) angle at its input terminals. However, the input currents drawn from the grid are not sinusoidal. The high-frequency ripples are suppressed by input current filters (ICFs).These filters additionally introduce a leading phase angle for the current which varies with the loading. This phase lead can be compensated by adjusting the angle between the input current space vector and the input voltage space vector of the MC. The computation of this adjustment angle depends on the estimation of power losses in the switching devices. A simple method is proposed in this paper to estimate the switching losses without measuring device voltages and currents using the perturbation technique. The perturbation logic depends on input current, instantaneous active and reactive power computed at regular intervals of time. The proposed method effectively minimises the IDPF angle very close to zero. The experimental results are included for validation,

Keywords: *matrix converter • input current filter • input power factor angle • input displacement factor • switching losses*

1. Introduction

In the family of AC–AC power frequency conversion systems, the topology of three phase to three phase direct matrix converter (MC) as shown in Figure 1 has certain advantageous features namely: (1) independent control of output voltage magnitude and frequency, (2) no requirement of bulky and expensive energy storage elements, (3) input displacement power factor (IDPF) control and (4) bidirectional power flow capability. These attractive advantageous features make the MC a potential candidate as a power frequency changer for various industrial applications such as variable frequency drives (Basak et al., 2016; Mondal and Kastha, 2015), wind power extraction (Mondal and Kastha., 2017; Sofiane et al., 2019) and distributed power generation system (Liu et al., 2013), etc.

The MC output current becomes nearly sinusoidal inherently due to the inductive load, whereas high-frequency components present in its input currents are due to the space vector pulse width modulation (SVPWM) of power semiconductor switching devices at very high switching frequency. The input currents entering the MC are i_{am}, i_{bm} and i_{mc} for the phases a, b and c, respectively. Normally LC–type second-order input current filter (ICF) is used to mitigate these high-frequency components from input currents drawn from the grid (Dasgupta and Sensarma, 2014; Kume et al., 2007; Popovici and Mutiu 2021). The ac currents drawn from the AC grid are i_{ai}, i_{bi} and i_{ci} for the phases a, b and c, respectively. The ICF is identified in Figure 1. The inductor is represented by its equivalent series resistance (ESR)'r' and inductance 'L_f'. To prevent the high voltage from appearing across the inductor when its current is interrupted, a non-inductive resistor 'R_d' is put across the inductor.The filter capacitors are identified

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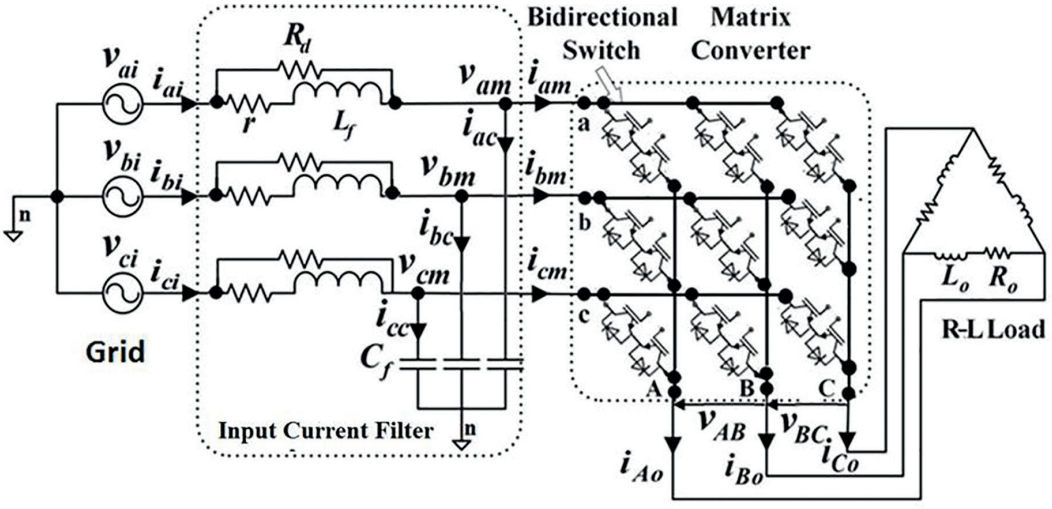


Fig. 1. Power schematic diagram of three phase to three phase direct MC with ICF. ICF, input current filter; MC, matrix converter.

as 'C_f'. Two IGBTs are used to realise the bidirectional switches as shown in Figure 1. Even though the MC can be controlled to have unity displacement power factor (UDPF) at its input terminals i.e. the grid frequency component of the current can be maintained in same phase as the grid frequency component of the respective phase voltage at the input terminals of the MC, this ICF causes an unwanted leading phase shift in the AC grid side current (Kume et al., 2007). It is not possible to neutralise the effect with the ICF design (Xian-hui et al., 2014); hence different control schemes are evolved to maintain nearly UDPF at AC grid side (Das et al., 2018; Gong et al., 2019; Hamouda et al., 2016; Huber and Borojevic, 1995; Kwak and Toliyat, 2003; Lu et al., 2009; Milanovic and Dobaj, 2000; Nguyen et al., 2011).

It is mentioned in Huber and Borojevic (1995) that the IDPF angle at the input of the MC should be adjusted to get nearly UDPF at the utility(grid) side depending on the loading condition. The algorithm to get the required phase angle compensation is not clearly discussed. For a direct MC, a combined symmetrical and asymmetrical modulation method is proposed in Milanovic and Dobaj (2000) to achieve UDPF operation at the utility side. In this method, the mathematical relationships are developed by considering the input-output power balance of the MC. The method is complex and requires the estimation of reactive power demand of the load.The method does not consider the losses of MC and its other circuitry. To provide accurate dynamic compensation of the IDPF angle, a closed-loop decoupled current control scheme is proposed in Kwak and Toliyat (2003). Here, independent control of the active and reactive components of current is achieved by designing the control equations in rotating d–q reference frame. The method depends on the estimation of ICF parameters, power delivered to load and estimation of losses in MC and its circuitry. A PI controller is used and the method to determine the gains of the controller is not discussed. The experimental results are not available. The method described by Lu et al. (2009) depends on the calculation of the required angle between input current space vector and the voltage space vector to achieve nearly IDPF at the utility (grid) side. The method depends on values of the circuit parameters of the ICF and loading conditions. The losses in the MC and the ICF are neglected. In Nguyen et al.(2011), two IDPF angle compensation methods are proposed. The first methodis basically similar to the compensation technique proposed in Lu et al.(2009) considering the direct modulation of the switching pulses and the second one proposes a closed-loop PI regulator-based control algorithm to overcome the parameter dependence of the first method. This method provides satisfied dynamic performance but requires two phase locked loop (PLL), one for voltage and another for current to obtain the utility (grid)-side displacement power factor angle (UDPFA) i.e. the phase angle between the utility (grid) sinusoidal phase voltage and the corresponding sinusoidal phase current drawn from the utility (grid). After getting the information of UDPFA, the PI controller-based closed-loop control strategy becomes effective in regulating the IDPF angle of MC. In Hamouda et al. (2016), the method to maintain UDPF at the grid side in presence of unbalanced voltage for an indirect MC (IMC) is elaborated with experimental results. The method depends on accurate estimation of the reactive parameters of the ICFs. The PIR controller is used instead of PI controller to determine the input current reference of the IMC. The variables are transformed into d–q synchronously rotating variables. The losses in the IMC are neglected. In Das et al.(2018), two methods were discussed. In the first method, the required input

reference current vector in d–q frame for the MC is found analytically. This method relies on the values of the ICF circuit parameters and does not take into account the losses in the converter and its associated circuit. In the second method, the angle of the input current vector of the MC is adjusted iteratively following a logic to get unity displacement factor at the grid side. Here the filter circuit parameters are not required and the losses in the MC and its associated circuit are implicitly considered. This does not discuss how the perturbation steps are to be determined to avoid instability. No experimental validation is found. In Gong et al. (2019), a low-cost closed-loop IDPF compensation scheme is proposed to reduce the cost compared to the existing closed-loop compensation methods for the IMC. The least mean square algorithm is used to generate a virtual voltage signal, the magnitude of which is equal to the grid voltage and the phase angle is reflected from the grid current by adaptive virtual resistance calculation. This virtual voltage generates error signal from the grid voltage, which is eventually regulated by the closed-loop PI controller to achieve UDPF operation at grid side. The method to select the gains of the controller is not discussed and requires processing the least mean square of the control variable.

The work reported in this paper is primarily based on the work in Das et al. (2018). The analytical solution to obtain the input current space vector is modified to take into account the losses in the direct MC. A perturbation technique is introduced to get iteratively the losses in the MC. Experimental results are provided.

In wind power generation,a power frequency changer is required to control the power flow between two sources of different frequencies in order to drive a doubly fed induction generator. This is generally realised by combining a pulse width modulated (PWM) rectifier with a PWM voltage source inverter (VSI) (Blecharz et al., 2017; Gajewski and Pieńkowski, 2016; Iwański and Łuszczyk, 2017). These two converters share a common DC bus. In this paper, the direct MC is modelled as a combination of a conceptual voltage source rectifier (VSR) and a conceptual VSI. The configuration is shown in Figure 2. The 12 switches in the model are ideal bidirectional switches.The input terminals of the conceptual VSR are connected to the three output terminals of the ICFs as shown in Figure 2. The output voltage of the conceptual VSR is a DC voltage (V_{DC}). This DC voltage is also the input DC bus voltage of the conceptual VSI. The output of the VSI gives desired three phase voltages.The DC bus current (I_{DC}) is a measure of the loading of the MC.The SVPWM for the generation of switching pulses is applied for conceptual switches of VSR and VSI separately. The pulses are then combined suitably to get the pulses for nine physical bi-directional switches made of 18 semiconductor switches (IGBTs) in the direct MC. The input of the direct MC with ICF is modelled in synchronously rotating (d–q) reference frame to estimate the ICF losses in terms of grid current and to generate reference input current space vector for the conceptual VSR part of the direct MC. A perturbation technique is used to take into account the losses in the MC switches and associated circuits. These loss terms are used in the power balancing principle to generate the desired virtual grid current (VGC) to achieve UDPF at the grid side. From this VGC, the input current space vector is computed for the VSR part of the MC. Here, the computations of instantaneous active power and reactive power at regular sampling instants are required to obtain the information of the grid side displacement power factor angle (GSDPFA) i.e. the phase angle between the grid sinusoidal phase voltage and the corresponding sinusoidal phase current drawn from the grid. Note that only one PLL is required to implement the scheme andthere is no requirement of any PI controller or PIR controller.

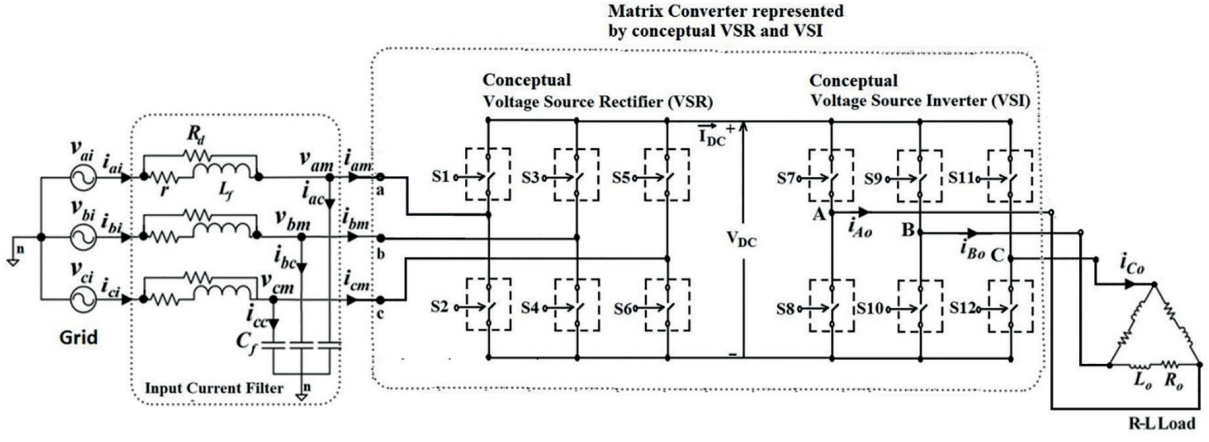


Fig. 2. Modified power schematic diagram of three-phase to three-phase direct MC. MC with nine bidirectional switches is replaced by the model of a direct MC consisting of conceptual VSR and conceptual VSI. MC, matrix converter; VSI, voltage source inverter; VSR, voltage source rectifier.

The work reported is structured as follows: The impact of ICF on MC performance is briefly discussed in Section 2. The MC modelling and modulation method are described briefly in Section 3. The proposed control scheme is described in Section 4. The experimental validation and discussions are presented in Section 5. The conclusions are given in Section 6.

2. Effects of ICF

The effects of ICF on MC can be explained through phasor diagrams. The phasors of different currents and voltages corresponding to phase-a in Figure 1 are drawn in Figure 3(a). As seen in the phasor diagram in Figure 3(a), the LC–type ICF in MC causes an undesired leading phase shift of 'ϕ_{ai}' in grid side current with respect to grid phase voltage '$\bar{V}_{ai}$' even though the input phase-a current ($\bar{I}_{am}$) into the MC is controlled to be in same phase with input phase-a voltage ($\bar{V}_{am}$) at the input 'a' terminal of the MC i.e. the IDPF angle (ϕ_{am}) at the input of the MCis equal to zero. So, the angle (ϕ_{am}) is to be made lagging to compensate this as shown in Figure 3(b). It is observed that the angle ϕ_{am} is not a fixed value, but depends on current drawn from grid which itself depends on loading of the MC.The compensation also affects the phase angle (δ_{ai}) between the phasor ($\bar{V}_{am}$) and the phasor $\bar{V}_{ai}$ as shown in Figure 3.

All the voltages here are referred to the grid neutral node 'n' as shown in Figure 1. The voltage drop caused by the ICF inductor's ESR is ignored. However, the phasor diagram takes into account the voltage drop across the equivalent series reactance of the ICF circuits' series branch. The current through the resistance 'R_d' is neglected in the phasor diagram.

3. Modelling of the Direct MC

As shown in Figure 2, the conceptual VSR consists of six bi-directional ideal switches and acts as a PWM VSR. The SVPWM scheme is employed to generate pulses for the six switches. Depending on the value of I_{DC}, the different stationary input current space vectors can be constructed for different allowable switching states. Table 1 shows the different active stationary input current space vectors.

The stationary active input current space vectors are shown in Figure 4.The circle touching the hexagon formed by the lines joining the tips of the space vectors sets the limiting boundary of the rotating reference input current space vector ($\vec{i}_m$). It can be shown that the space angle (φ_m) between the reference input current space vector ($\vec{i}_m$) and the input voltage rotating space vector ($\vec{v}_m$) determines the available DC link voltage (V_{DC}) at the output of the conceptual VSR. The expression of the output DC voltage is given in Eq. (1) Huber and Borojevic (1995).

$$V_{DC} = \frac{3}{2}.m_{VSR}V_{mph}.\cos\varphi_m \tag{1}$$

where m_{VSR} is the modulation index of the conceptual VSR and V_{mph} is the peak value of the AC input phase voltage at the input terminal of the direct MC. The modulation index (m_{VSR}) is kept ata constant value of unity. The DC voltage is a cosine function of φ_m. So, any deviation of φ_m from zero decreases the magnitude of the available DC voltage. This decrease in DC voltage causes a decrease in the available AC output voltage. The active stationary output line-to-line space vectors available from the different allowable switching states in the conceptual VSI are

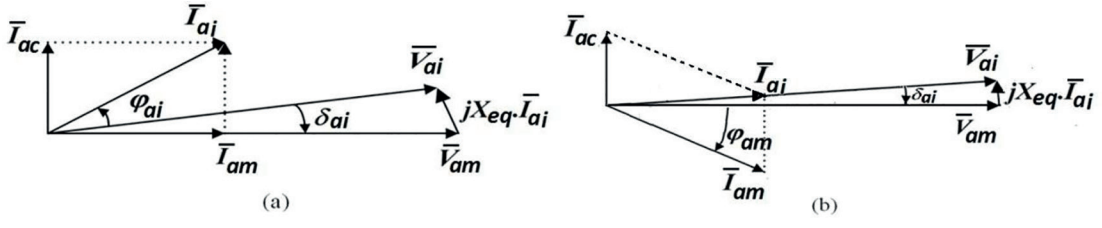


Fig. 3. (a) The non-zero IDPF angle under the impact of the ICF is shown in a phasor diagram. (b) Illustration with phasor diagram to show the adjustment by controlling the IDPF angle of the MC to modify the IDPF angle to be zero. ICF, input current filter; IDPF, input displacement power factor; MC, matrix converter.

Table 1. Different switching state active stationary input current space vectors.

Switching states $\begin{bmatrix} S1 & S3 & S5 \\ S4 & S6 & S2 \end{bmatrix}$	Magnitude, A	Angle, radian	Assigned name
$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\frac{2}{\sqrt{3}} I_{DC}$	$\frac{\pi}{6}$	$\vec{I}_1$
$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\frac{2}{\sqrt{3}} I_{DC}$	$\frac{\pi}{2}$	$\vec{I}_2$
$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}$	$\frac{2}{\sqrt{3}} I_{DC}$	$\frac{5\pi}{6}$	$\vec{I}_3$
$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$\frac{2}{\sqrt{3}} I_{DC}$	$-\frac{5\pi}{6}$	$\vec{I}_4$
$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}$	$\frac{2}{\sqrt{3}} I_{DC}$	$-\frac{\pi}{2}$	$\vec{I}_5$
$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$	$\frac{2}{\sqrt{3}} I_{DC}$	$-\frac{\pi}{6}$	$\vec{I}_6$

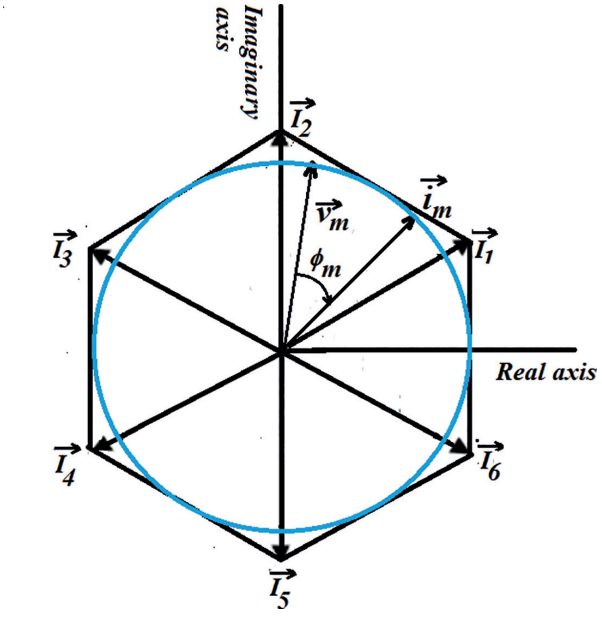


Fig. 4. Stationary active space vectors for the input current to the conceptual VSR. VSR, voltage source rectifier.

shown in Table 2. The active stationary space vectors are shown in Figure 5. The rotating space vector $\vec{v}_{oref}$ is the space vector representation of the desired output line-to-line voltage. The magnitude of this space vector for linear operation is expressed in Eq. (2)

$$\left|\vec{v}_{oref}\right| = m_{VSI} \times V_{DC} \tag{2}$$

where m_{VSI} is the modulation index for VSI and it can vary from zero to unity. It is apparent that the magnitude of the available output voltage depends on V_{DC}.

Depending on the angular position of the reference input current space vector in the input current space vector diagram (Figure 4), two enclosing nearest active stationary space vectors in some proportions are considered to

Table 2. Different switching state active stationary output line-to-line voltage space vectors.

Switching states $\begin{bmatrix} S7 & S9 & S11 \\ S8 & S10 & S12 \end{bmatrix}$	Magnitude, V	Angle, radian	Assigned name
$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\frac{2}{\sqrt{3}}V_{DC}$	$\frac{\pi}{6}$	$\vec{V}_{1LL}$
$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\frac{2}{\sqrt{3}}V_{DC}$	$\frac{\pi}{2}$	$\vec{V}_{2LL}$
$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}$	$\frac{2}{\sqrt{3}}V_{DC}$	$\frac{5\pi}{6}$	$\vec{V}_{3LL}$
$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$\frac{2}{\sqrt{3}}V_{DC}$	$-\frac{5\pi}{6}$	$\vec{V}_{4LL}$
$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}$	$\frac{2}{\sqrt{3}}V_{DC}$	$-\frac{\pi}{2}$	$\vec{V}_{5LL}$
$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$	$\frac{2}{\sqrt{3}}V_{DC}$	$-\frac{\pi}{6}$	$\vec{V}_{6LL}$

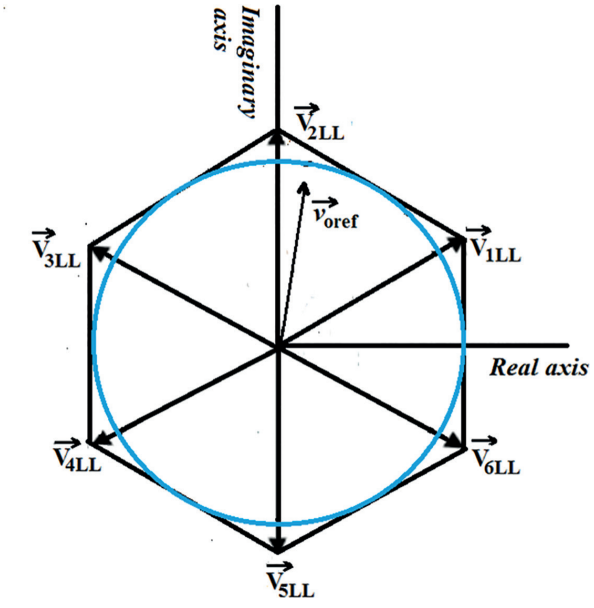


Fig. 5. Stationary active output line to line voltage space vectors for the conceptual VSI. VSI, voltage source inverter.

construct the input current space vector. The proportions of the chosen space vectors determine the duty ratio of the switches creating the stationary space vectors. Therefore, two active duty ratios are computed at each switching cycle interval.The remaining part of the switching cycle is assigned for the participation of the non-active stationary space vectors. Similarly, the duty ratios of switches in the conceptual VSI are determined depending on the position of the desired line-to-line output voltage in the output line-to-line voltage space vector diagram (Figure 5). The active duty ratios of the bi-directional semiconductor switches in the direct MC are found by suitably multiplying the duty ratios of VSR part and VSI part. The four combination products of the active duty ratios are thus obtained. The duty ratios of switches to give zero line to line output voltage are found by subtracting sum of the active duty ratios from unity (Huber and Borojevic, 1995). Since, bi-directional semiconductor switches are realised by two conventional IGBTs, altogether 18 switching pulses are generated for commutation purposes.

4. Minimisation of Input Power Factor Angle by Controlling MC IDPF Angle

The minimisation of input power factor angle is achieved by controlling the angle of the conceptual input current space vector (φ_m) with respect to the input voltage space vector for the VSR, whereas the modulation index of VSR is maintained unity to get the maximum DC-link voltage possible at any angle of the input current space vector. In this section, the proposed compensation scheme is described. In this method, the required reference current vector for VSR part is computed directly using a new method of estimating the power loss in MC and its associated circuit.

The proposed control scheme uses the instantaneous active power balancing principle to compute the input current vector of MC. The instantaneous active power drawn from the grid must be equal to the instantaneous power loss in the ICF, power losses in the semiconductor switches of the MC, the power losses in the protective clamp circuit and the active power delivered to the load. It is very difficult to estimate the power losses in the MC switches and protective clamp circuit at every sampling instant. The requirement of instantaneous active power components is computed in a d–q synchronously rotating reference frame. The input grid voltage is aligned with the d-axis. It is further assumed that the reference input current vector at the grid end is aligned with the input voltage vector to maintain UDPF at the grid terminals. The equivalent circuitis shown in Figure 6. The d–q synchronously rotating reference frameis used to represent electrical circuit connecting grid, ICF and input of the direct MC. The output electrical circuit is represented in the stationary A–B–C frame. The d–q synchronously rotating reference frame is used to compute the reference input current vector to generate SVPWM pulses for the conceptual VSR part of the direct MC.

4.1. Modelling of ICF in d–q reference frame

The ICF can be modelled in synchronously rotating (d–q) reference frame (Das et al., 2018). The grid voltage space vector is oriented along the d-axis. The reference q-axis component of grid current is zero to minimise the input power factor angle. Eqs (3) and (4) are used where the subscript {*} indicates the desired quantities.

$$i^*_{Rq}R_d = i^*_{Lq}r + L_f\frac{di^*_{Lq}}{dt} + \omega_i L_f i^*_{Ld} \tag{3}$$

$$i^*_{Rd}R_d = i^*_{Ld}r + L_f\frac{di^*_{Ld}}{dt} - \omega_i L_f i^*_{Lq} \tag{4}$$

$$i^*_{id} = i^*_{Rd} + i^*_{Ld} \tag{5}$$

$$i^*_{iq} = i^*_{Rq} + i^*_{Lq} \tag{6}$$

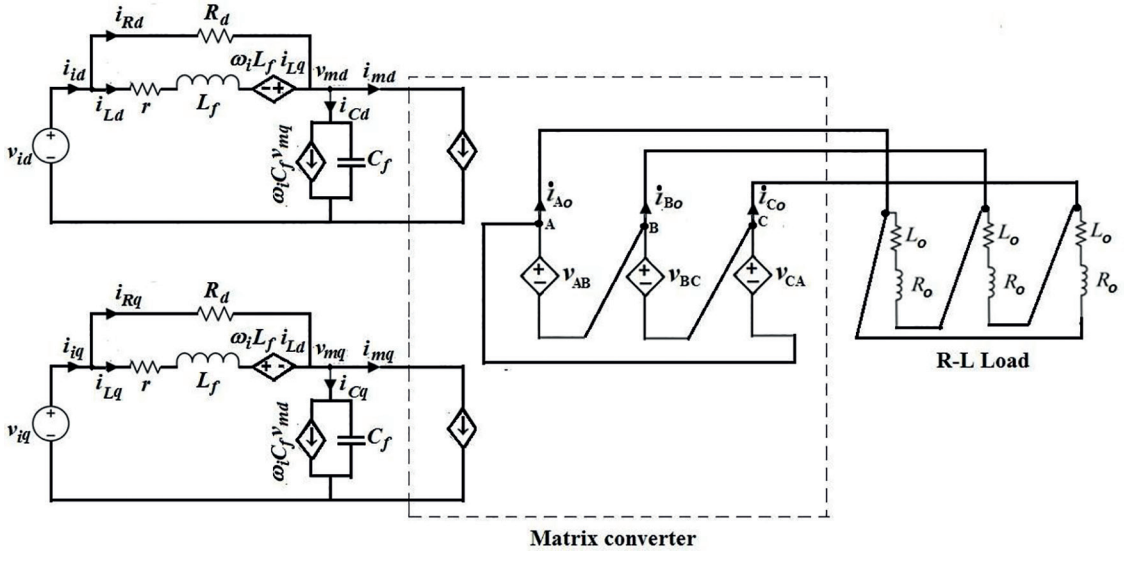


Fig. 6. Three phase equivalent circuit representation of ICF in d–q reference frame in conjunction with direct MC and its load. ICF, input current filter; MC, matrix converter.

Neglecting the derivative terms at steady state, the Eqs (3) and (4) are rewritten as in Eqs (7) and (8), respectively.

$$i^*_{Rq}R_d = i^*_{Lq}r + \omega_i L_f i^*_{Ld} \tag{7}$$

$$i^*_{Rd}R_d = i^*_{Ld}r - \omega_i L_f i^*_{Lq} \tag{8}$$

4.2. Estimation of instantaneous active power consumption in ICF

Losses in the ICF are obtained by computing the current through the damping resistance and inductor. Using Eqs (3)–(6), these currents at steady state are expressed in Eqs (9)–(12).

$$i^*_{Rq} = -i^*_{Lq} \text{ (as } i^*_{iq} \text{ should be zero)} \tag{9}$$

$$i^*_{Lq} = -\frac{\omega_i L_f}{(R_d + r)} i^*_{Ld} \tag{10}$$

$$i^*_{Rd} = \left(\frac{r(R_d + r) + (\omega_i L_f)^2}{(R_d + r)^2 + (\omega_i L_f)^2} \right) \cdot i^*_{id} \tag{11}$$

$$i^*_{Ld} = \left(\frac{R_d(R_d + r)}{(R_d + r)^2 + (\omega_i L_f)^2} \right) \cdot i^*_{id} \tag{12}$$

4.3. Calculation of the instantaneous active power and reactive power at grid side

The instantaneous active power (p) and instantaneous reactive power (q) are computed using Eqs (13) and (14).

$$p = v_{ai}i_{ai} + v_{bi}i_{bi} + v_{ci}i_{ci} \tag{13}$$

$$q = 0.577\ \left[(v_{bi} - v_{ci})i_{ai} + (v_{ci} - v_{ai})i_{bi} + (v_{ai} - v_{bi})i_{ci}\right] \tag{14}$$

4.4. Power balance equation

The instantaneous active power drawn from the grid must be equal tosummation of the instantaneous active power delivered to the output AC load, the losses in the ICF and the losses in the MC and its associated circuitry. At each sampling instant, this can be utilised to get estimated losses in the MC and its associated circuits.

$$v_{id} \cdot i^*_{id} = p_0 + p_{MC} + {i^*_{Ld}}^2 \cdot r + {i^*_{Rd}}^2 \cdot R_d \tag{15}$$

In Eq. (15), p_{MC} is the estimated loss in the MC and its associated circuits.

4.5. Estimation of MC-related losses

MC losses include switching loss and conduction loss of its switches and losses in the over-voltage protection circuits. The accurate compensation of IDPF angle cannot be estimated without considering the MC-related losses. To avoid a complex estimation method for the losses, the perturbation technique is used to estimate the losses. The instantaneous active power and reactive power are computed from the input grid currents and input grid voltages at each sampling instantusing Eqs (13) and (14), respectively. The displacement power factor angle at the grid terminal (GSDPFA) (φ_i) is computed at each sampling instant utilising and q.The calculation of the angle at a particular sampling instant is illustrated in Figure 7. As illustrated in Figure 8, by comparing the values of φ_i at the sampling instant with the previous sample, a small and fixed value as a measure of MC internal losses is added or subtracted, depending on values of $i^*_{id}(k-1)$ and $i^*_{id}(k)$, to the power balance equation in Eq. (15) to estimate the i^*_{id} for the next sampling instant. This estimated i^*_{id} is used to compute the input current space

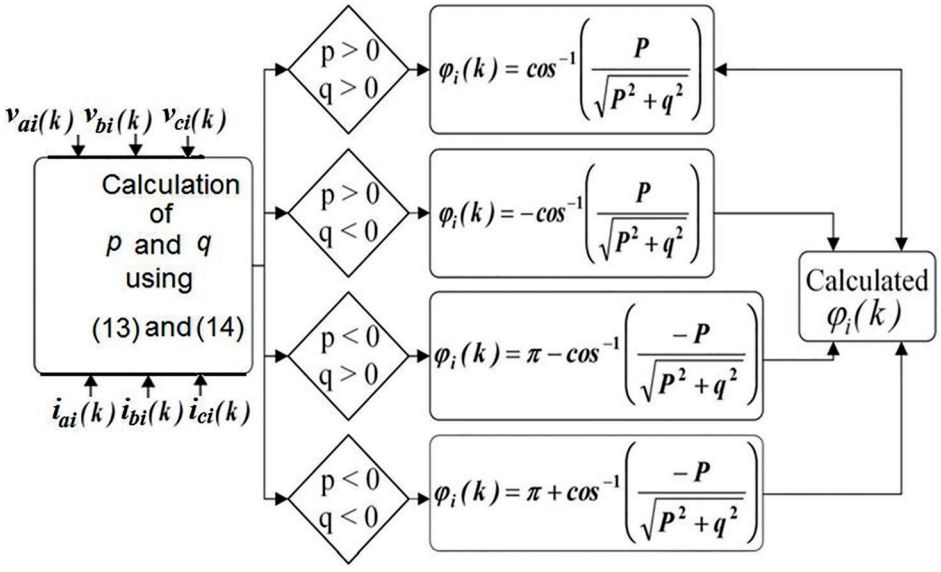


Fig. 7. Computation of GSDPFA at each sampling instant. GSDPFA, grid side displacement power factor angle.

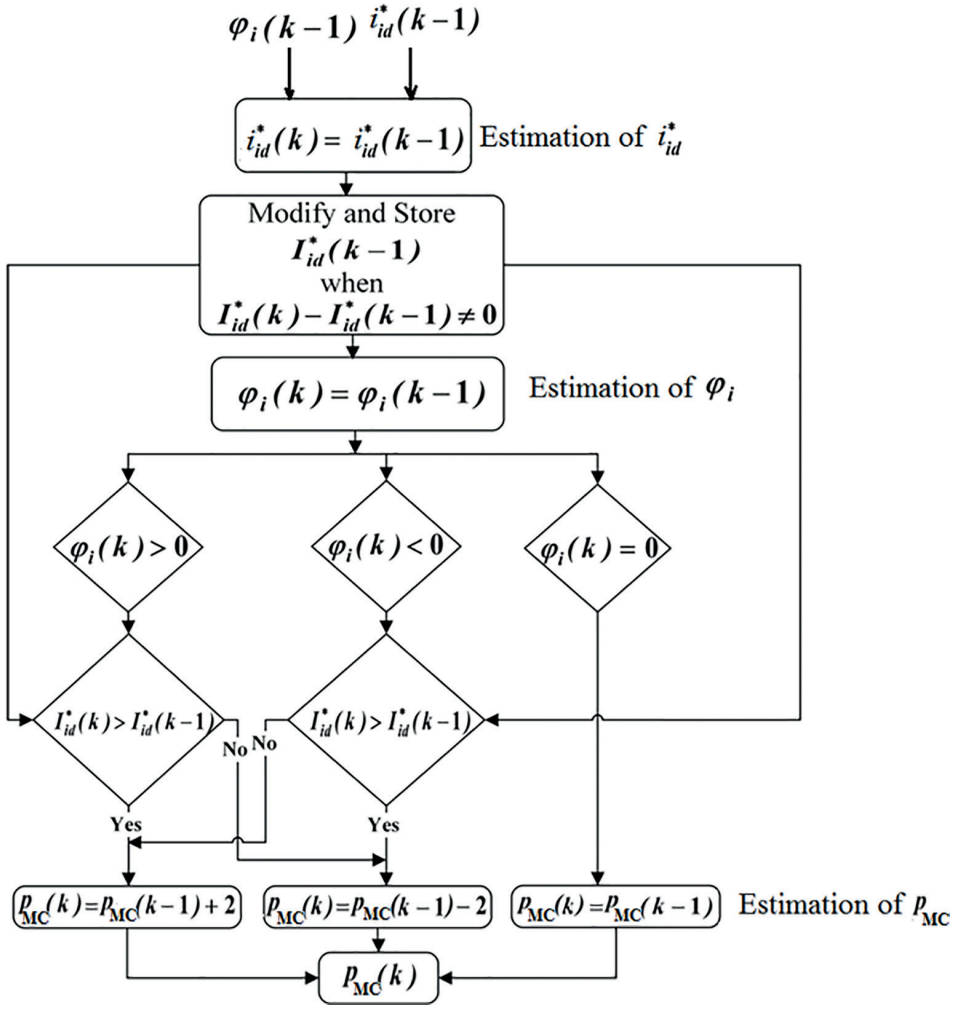


Fig. 8. Estimation of internal power losses of MC and its circuit. MC, matrix converter.

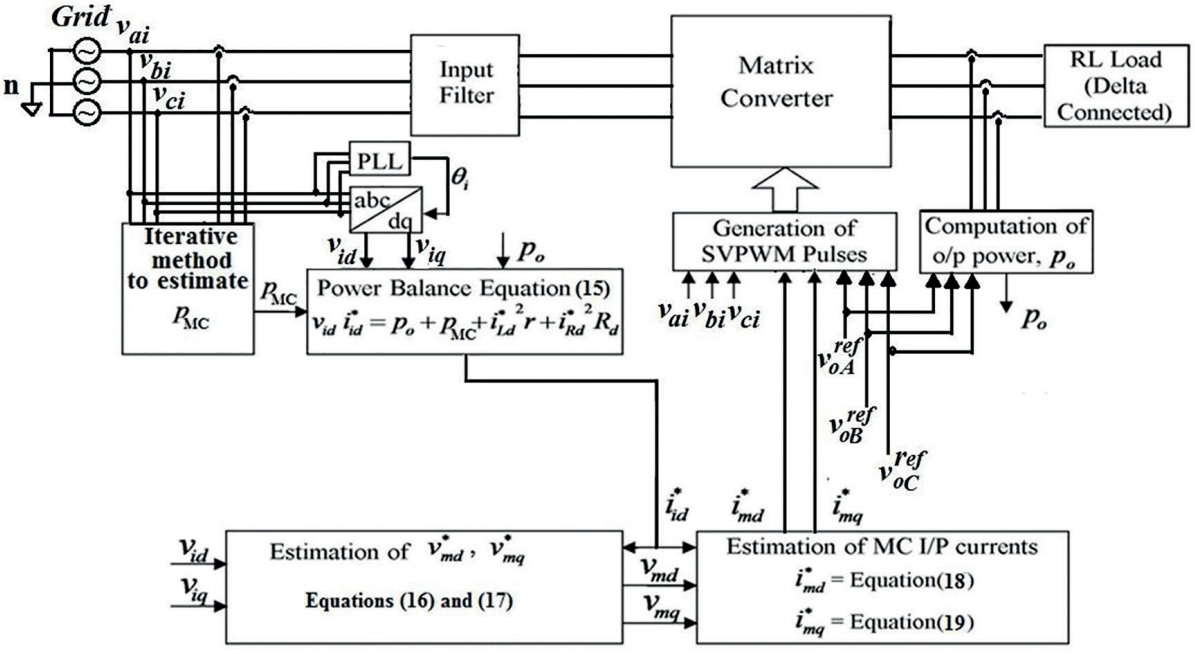


Fig. 9. Entire scheme of the proposed method. MC, matrix converter; PLL, phase locked loop; SVPWM, space vector pulse width modulation.

vector ($\vec{i}_m$) of the VSR part of the direct MCusing Eqs(16)–(19). With this $\vec{i}_m$, the duty ratios of the switches in the conceptual VSR are computed. The duty ratios of the switches of the conceptual VSI are computed utilising the reference output line to line voltage space vector $\vec{v}_{oref}$. After this, the output power at the sampling instant is calculated. These values are used to estimate losses in the MC for the next iteration. Thus, the process always seeks the minimum input power factor angleby achieving φ_i to be zero. The entire scheme of the proposed method is illustrated in Figure 9.

4.6. Computation of the input current reference space vector for conceptual VSR

$$v^*_{md} = v^*_{id} - \left(\frac{r(R_d + r) + (\omega_i L_f)^2}{(R_d + r)^2 + (\omega_i L_f)^2} \right) \cdot i^*_{id} R_d \tag{16}$$

$$v^*_{mq} = v^*_{iq} - \left(\frac{R_d \omega_i L_f}{(R_d + r)^2 + (\omega_i L_f)^2} \right) \cdot i^*_{id} R_d \tag{17}$$

$$i^*_{md} = i^*_{id} - \left(C_f \frac{dv^*_{id}}{dt} - \omega_i C_f v^*_{mq} \right) \tag{18}$$

$$i^*_{mq} = -\left(C_f \frac{dv^*_{iq}}{dt} + \omega_i C_f v^*_{md} \right) \tag{19}$$

Since the voltage drop across the filter series branch is negligible, the reference voltages v^*_{mq} and v^*_{md} can be equated with the corresponding voltage components at the grid terminal. Also, at steady state, the derivative terms can be neglected. Due to the filter capacitor, the magnitude of the i^*_{mq} is not zero, but a negative value. This indicates, that the current space vector at the input terminal of the direct MC stays behind the input voltage space vector to achieve UDPF at the grid side.

5. Experimental Results

The electrical parameters of the ICF and load parameters are given in Table 3. For experimental validation, a SEMIKRON make 25 kVA direct MC stack is used. The additional circuits are developed in the laboratory. The experimental setup is shown in Figure 10, where, the entire control logics are realised in FPGA (EP1C12Q240C8) platform. The diode bridge clamp circuit for over voltage protection and the four-step current commutation scheme based on the direction of output current are realised to protect against open circuits at the load end and short circuits between input phases respectively.

The iteration process to determine the losses in the direct MC and its associated circuit considered 2 watts for the losses at the start of initial iteration. The LEM LV 25P voltage sensors are used to step down and isolate the voltages at the grid terminals for observing the waveform through YOKOGOWA 4 channel DSOand Tektronix TBS 1062 DSO.YOKOGWA 1000:1 V/V differential probe is used for sensing the output line to line voltages. Similarly, the HONEYWELL CSNE151 current sensors are used to get isolated voltage proportional to the currentfor observing the waveform through YOKOGOWA 4 channel DSO.The experimental results for the phase-a voltage and phase-a current without compensation at steady state are shown in Figure 11. The time scale extended view near negative to positive going zero crossing of the voltage and current is shown in Figure 11(b). It shows that the input current is leading the corresponding input phase voltage by a small amount of 10.8°. The experimental results for the phase-a voltage and phase-a current with compensation

Table 3. Parameters for ICF and output load.

Parameter	Values
L_f	0.78 mH
r	1.2 Ω
R_d	120 Ω
C_f	9 μF
R_o	20 Ω
L_o	50 mH

ICF, input current filter.

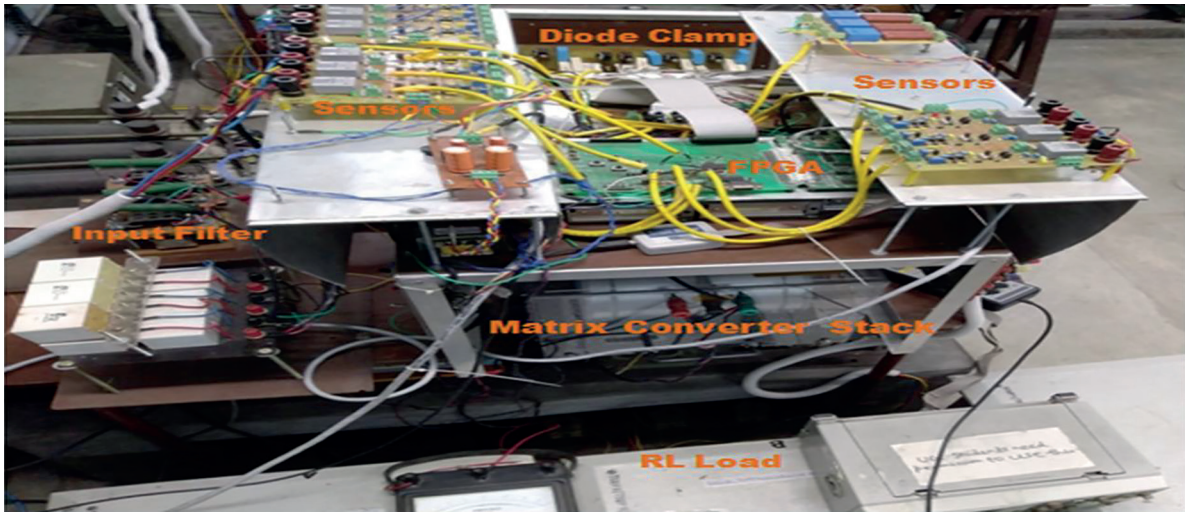
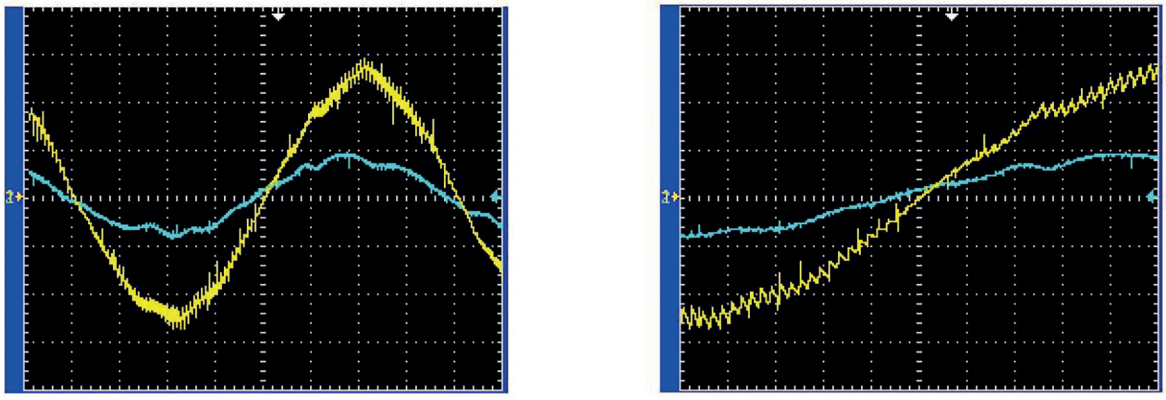
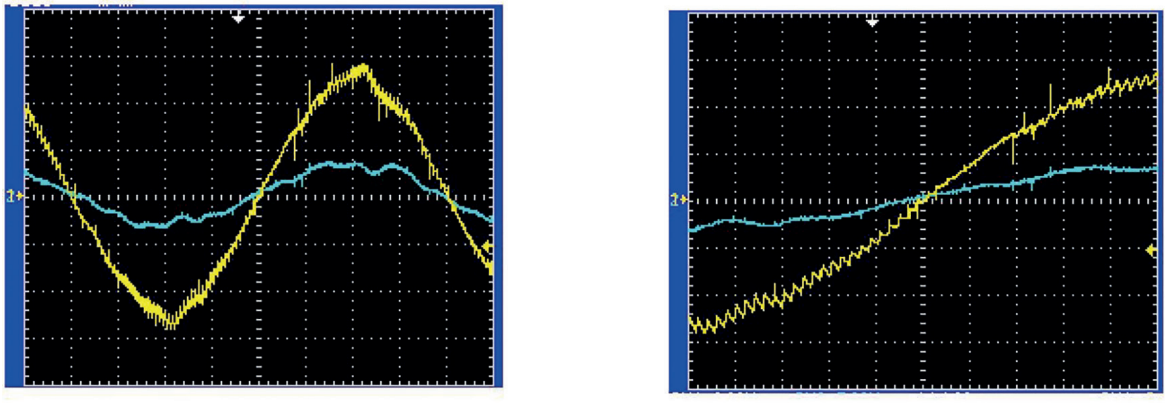


Fig. 10. Experimental set-up.



(a) (b)

Fig. 11. The steady-state experimental results without compensation: (a) Vertical axis: 101 V/div for voltage and 3.42A/div for current, Horizontal axis: 2.5 ms/div. Yellow trace: Grid phase-a voltage, Blue trace: Grid phase-a current, (b) Time scale expanded view near positive going zero crossing of the voltage and current: Vertical axis: 101 V/div for voltage and 3.42 A/div for current, Horizontal axis: 1 ms/div.Yellow trace: Grid phase-a voltage, Blue trace: Grid phase-a current, Switching frequency: 5 kHz, Input three phase AC voltage: 346 V, 50 Hz, Modulation index: 0.26, output frequency: 20 Hz, output R-L load: L = 50mH and R = 20 Ω.



(a) (b)

Fig. 12. The steady-state experimental results with compensation: (a) Vertical axis: 101 V/div for voltage and 3.42 A/div for current, Horizontal axis: 2.5 ms/div. Yellow trace: Grid phase-a voltage, Blue trace: Grid phase-a current, (b) Time scale expanded view near positive going zero crossing of the voltage and current: Vertical axis: 101 V/div for voltage and 3.42 A/div for current, Horizontal axis: 1 ms/div.Yellow trace: Grid a-phase voltage, Blue trace: Grid a-phase current, Switching frequency: 5 kHz, Input three phase AC voltage: 346 V, 50 Hz, Modulation index: 0.26, output frequency: 20 Hz, output R-L load: L = 50 mH and R = 20 Ω.

at steady state are shown in Figure 12. The time scale extended view near positive going zero crossing of the voltage and current is shown in Figure 12(b), which shows that the phase angle between the phase current with respect to the corresponding phase voltages at the grid becomes zero with the application of the proposed scheme. Figures 13 and 14 show the voltage and current for two input phases after compensation and the expected magnitude and pattern of the output voltage and current, respectively. The modulation index is kept at 0.26 for the VSI part of the direct MC andthe output frequency is 20 Hz. The input AC line-to-line voltage is 346 V, 50 Hz.

5.1. Inspections of the system dynamics

The dynamic behaviours of the proposed method are verified through experiment. In Figure 15, load variation is obtained by using a step change of modulation index from 0.25 to 0.37. Within a very short time, the control action adjusts the displacement power factor angle to zero. It is clear that the proposed method provides satisfactory performance under steady state as well as in transient operation.

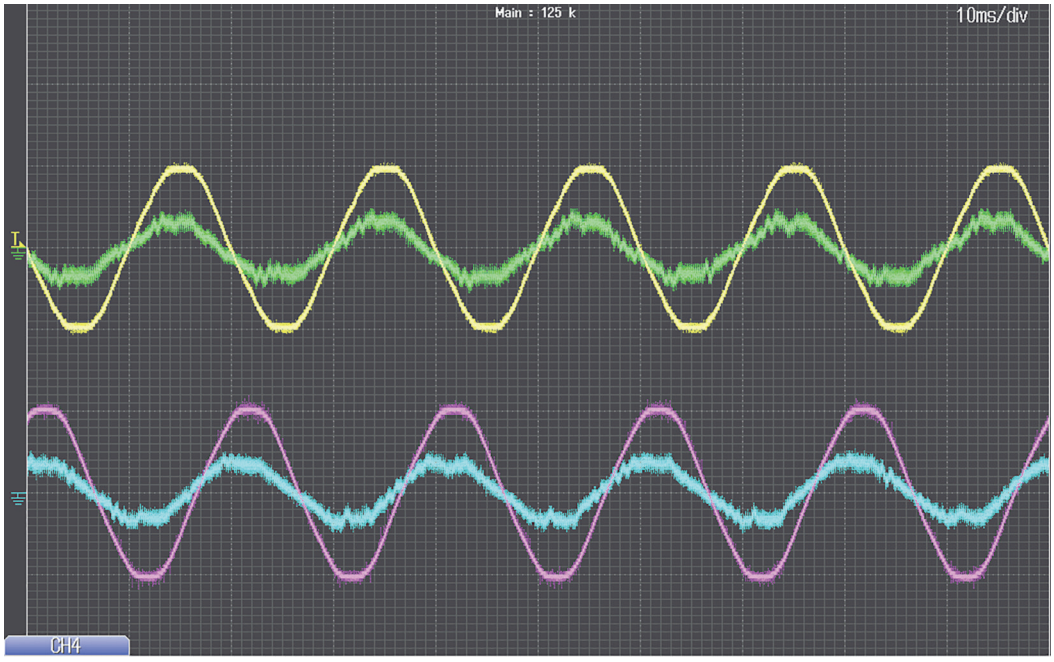


Fig. 13. The steady-state experimental results with compensation: Vertical axis: 283 V/div for voltage and 7 A/div for current, Horizontal axis: 10 ms/div. Yellow trace: Grid phase-a voltage, green trace: Grid phase-a current, Purple trace: Grid phase-b voltage, blue trace: Grid phase-b current waveform. Switching frequency: 5 kHz, Input three phase AC voltage: 346 V, 50 Hz, Modulation index: 0.26, output frequency: 20 Hz, output R-L load: L = 50 mH and R = 20 Ω.

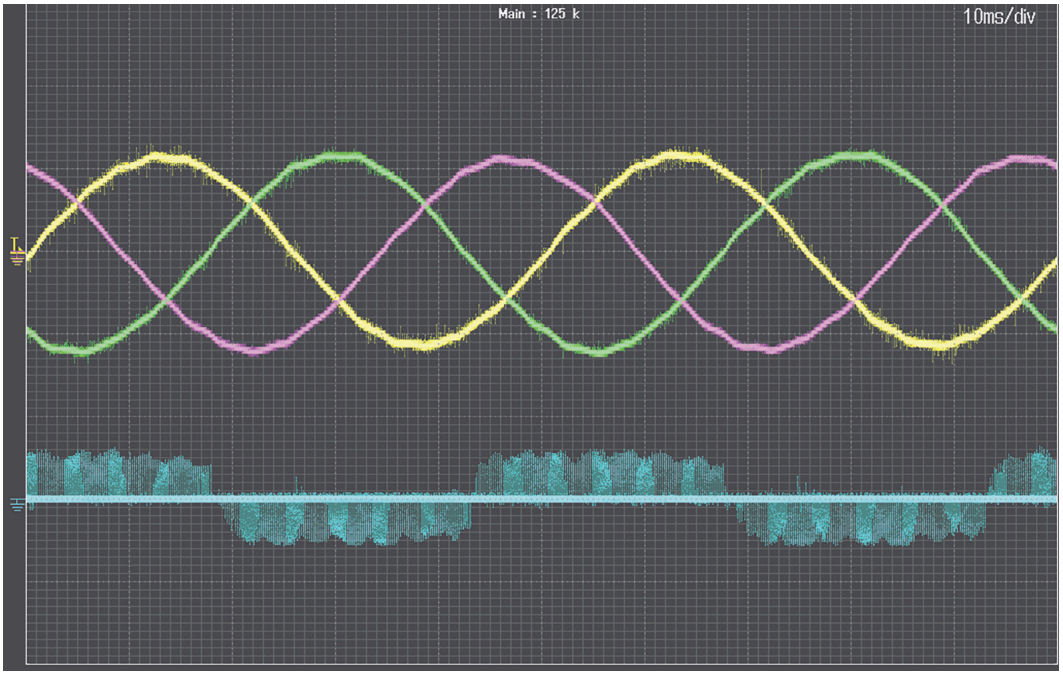


Fig. 14. The steady-state experimental results with compensation: Vertical axis: 1,000 V/div for voltage and 5 A/div for current, Horizontal axis: 10 ms/div. Yellow trace: Output phase-A line current, greentrace: Output phase-B line current, purple trace: Output phase-C line current, Blue trace: Output line-to-line voltage. Switching frequency: 5 kHz,Input three phase AC voltage: 346 V, 50 Hz, Modulation index: 0.26, output frequency: 20 Hz, output R-L load: L = 50 mH and R = 20 Ω.

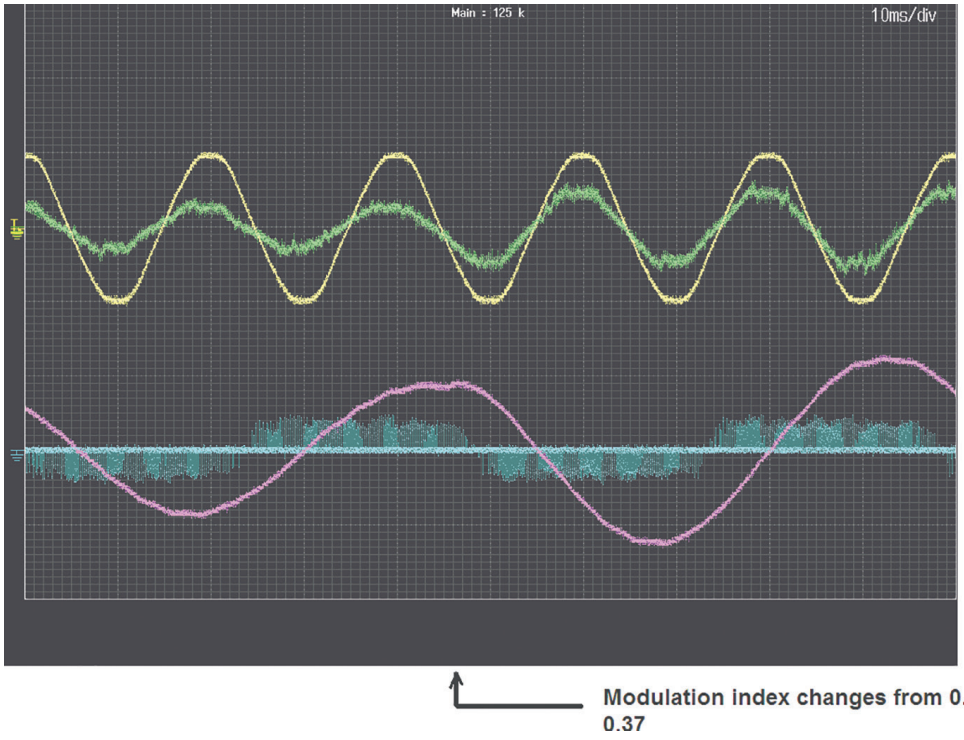


Fig. 15. The steady-state experimental results with compensation: Horizontal axis: 10 ms/div, Input voltage and current; Vertical axis: 8 A/div for current and 283 V/div for voltage, Yellow trace: Input A-phase voltage Input phase-a current, Output voltage and current; Vertical axis: 6 A/div for current and 1,000 V/div for voltage, purple trace: Output phase-A line current,Bluetrace: Output line-to-line voltage. Output frequency is 20 Hz. Switching frequency: 5 kHz, Input three phase AC voltage: 346 V, 50 Hz, Modulation index: 0.25 to 0.37, output frequency: 20 Hz, output R-L load: L = 50 mH and R = 20 Ω.

6. Conclusion

This paper has presented a method to minimise input power factor angle from the grid for a direct MC. In the demonstrated method, the MC reference input current for SVPWM is estimated using the power balance method. Nearly UDPF operation at the grid side is achieved by computing all losses accurately at every sampling instant. The ICF losses are computed in terms of grid side d-axis current whereas the MC losses are predicted using the perturbation method. Only one PLL is required for this method.The method is applicable only for three phase balanced condition. Further study is required to improve this method for application in unbalanced operation of the system.

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